REMARKS

By the present amendment and response, independent claims 1 and 12 and dependent claims 2, 8, and 16 have been amended to overcome the Examiner's objections. Claims 1-3 and 5-19 are pending in the present application. Reconsideration and allowance of pending claims 1-3 and 5-19 in view of the following remarks are requested.

The Examiner has rejected claims 1-3 and 5-19 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,963,810 to Gardner et al. ("Gardner") and further in view of U.S. patent number 6,124,158 to Dautartas et al. ("Dautartas"), U.S. patent number 5,994,192 to Chun-Yao Chen ("Chen") and "admitted prior art." For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 12, is patentably distinguishable over Gardner, Dautartas, and Chen, singly or in any combination thereof.

The present invention, as defined by amended independent claims 1 and 12, teaches, among other things, depositing a first ultra-thin nitride film on a semiconductor substrate, which comprises a silicon-on-insulator (SOI) wafer (claim 12), by atomic layer deposition, depositing a high-k material, which comprises a thin metal film comprising at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti), on the first ultra-thin nitride film, depositing a second ultra-thin nitride film on the high-k material by atom layer deposition, and "depositing a thick gate material on the second ultra-thin nitride film," "wherein the first and second ultra-thin

nitride films prevent the at least one material selected from the group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti) from diffusing into the semiconductor substrate and the thick gate material, respectively." As disclosed in the present application, the present invention provides a nitride/high-k material/nitride gate dielectric stack, where each nitride film is deposited by atomic layer deposition to achieve a thickness in a range of 1-2 atomic layer(s), and a gate electrode comprising a thick gate material, which is formed over the gate dielectric stack. As disclosed in the present application, the high-k material can comprise a thin metal film, which can comprise at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta).

As a result, the present invention achieves a high-k dielectric gate insulator where the first and second nitride films advantageously prevent the at least one metal selected from the group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta) from diffusing into the semiconductor substrate and the thick gate material, respectively, during subsequent high temperature processes. Thus, the present invention advantageously achieves a high-k dielectric gate insulator having good thermal stability. Additionally, the present invention achieves a high-k dielectric gate insulator that advantageously provides a reduction of direct tunneling current flow in a semiconductor device, such as a MOSFET.

In contrast to the present invention as defined by amended independent claims 1 and 12, Gardner, Dautartas, and Chen do not teach, disclose, or suggest depositing a first

ultra-thin nitride film on a semiconductor substrate, which comprises a silicon-on-insulator (SOI) wafer (claim 12), by atomic layer deposition, depositing a high-k material, which comprises a thin metal film comprising at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti), on the first ultra-thin nitride film, depositing a second ultra-thin nitride film on the high-k material by atom layer deposition, and "depositing a thick gate material on the second ultra-thin nitride film," "wherein the first and second ultra-thin nitride films prevent the at least one material selected from the group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti) from diffusing into the semiconductor substrate and the thick gate material, respectively." Gardner specifically discloses forming high permittivity layer 305 over thin nitride layer 303 and forming a nitride capping layer over high permittivity layer 305 prior to forming gate electrode layer 307. See, for example, column 5, lines 52-52, column 6, lines 13-15, and Figure 3C of Gardner.

In Gardner, nitrogen-bearing layers, i.e. thin nitride layer 303 and the nitride capping layer, formed between high permittivity layer 305 and the substrate or gate electrode layer 307 serve to inhibit oxidation of high permittivity layer 305 during subsequent processing. See, for example, Gardner, column 5, lines 13-24. In Gardner, the nitride capping layer may inhibit the diffusion of dopants (used to dope gate electrode layer 307) into high permittivity layer 305. However, Gardner fails to teach, disclose, or suggest forming thin nitride layer 303 and nitride capping layer by using atomic layer deposition. Additionally, Gardner fails to teach, disclose, or suggest forming thin nitride

layer 303 and the nitride capping layer to prevent at least one material selected from the group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti) from diffusing into the substrate and gate electrode layer 307, respectively. Further, Gardner fails to teach, disclose, or suggest depositing a high-k material, which comprises a thin metal film comprising at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti), on a thin nitride layer. Moreover, Gardner fails to teach, disclose, or suggest a substrate comprising a silicon-on-insulator (SOI) wafer, as required in amended independent claim 12.

Dautartas specifically discloses an atomic layer deposition process that is particularly advantageous for deposition of gate dielectric materials, such as aluminum oxide, from organic precursors, particularly trimethyl aluminum, as well as other dielectrics deposited from carbon-containing precursors, such as tantalum oxide from tantalum alcoholate. See, for example, Dautartas, column 3, lines 7-14. In Dautartas, a "sub-monolayer" of protection material, such as silicon dioxide, silicon oxynitride or silicon nitride can be formed over a silicon substrate such that the protection material does not completely cover the surface of the silicon substrate. See, for example, Dautartas, column 7, lines 5-17. In Dautartas, the sub-monolayer is a barrier to the formation of silicon monoxide but does not prevent treatment of the silicon substrate surface to form hydroxyl groups, which are utilized for depositing an aluminum oxide gate dielectric layer utilizing a trimethyl aluminum reactant. See, for example, Dautartas, column 5, lines 21-37 and column7, lines 5-14.

However, Dautartas fails to teach, disclose, or suggest forming first and second thin nitride layers to prevent at least one material selected from the group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti) from diffusing into the substrate and gate electrode layer, respectively. Further, Dautartas fails to teach, disclose, or suggest depositing a high-k material, which comprises a thin metal film comprising at least one material selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), and titanium (Ti), on a thin nitride layer. Moreover, Dautartas fails to teach, disclose, or suggest a substrate comprising a silicon-on-insulator (SOI) wafer, as required in amended independent claim 12.

Chen is cited by the Examiner to disclose using a photoresist as part of the patterning process as required in claims 10 and 18-19. However, Chen fails to cure the deficiencies of Gardner and Dautartas discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 12, is not suggested, disclosed, or taught by Gardner, Dautartas, and Chen, singly or in combination. As such, amended independent claims 1 and 12 are patentably distinguishable over Gardner, Dautartas, and Chen. Thus claims 3 and 4-11 depending from amended independent claim 1 and claims 13-19 depending from amended independent claim 12 are, *a fortiori*, also patentably distinguishable over Gardner, Dautartas, and Chen for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 12, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-3 and 5-19 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-3 and 5-19 pending in the present application is respectfully requested.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

James Gonko

James Gonko, Esq.
Reg. No. 45, 568

Date: 1/21/2004

James Gonko, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Telephone: (949) 784-4600
Facsimile: (949) 784-4601

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop RCE, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: 1/21/04

Sukhie Bal
Name of Person Mailing Paper and/or Fee

Signature 1/21/04
Date